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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,708	03/15/2004	Meng-Jyh Lin	LINM3016/EM	8974

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BACON & THOMAS, PLLC  
625 SLATERS LANE  
FOURTH FLOOR  
ALEXANDRIA, VA 22314

EXAMINER
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NGUYEN, LONG T

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No. 10/799,708	Applicant(s) LIN, MENG-JYH	
	Examiner Long Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 July 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-4,6 and 7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,6 and 7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)     | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Objections*

1. Claims 1-4 and 6-7 are objected to because of the following informalities:

Claim 1, line 7, "between" should be changed to --to--.

Claim 1, line 7, "the two pairs" should be changed to --the at least one transistor pair and the other resistor of the resistor pair-- so that the claim is clear.

Claim 1, it is suggested that the recitation "wherein the comparator has a detection voltage level" on line 10 be changed to --wherein the first comparison voltage has a detection voltage level--; and the recitation "varying with the detection voltage level" on line 11 be changed to --is selected based on the difference between the first and second comparison voltages-- to avoid misdescriptive problem in the claim since the first comparison voltage is the voltage to be detected (see lines 18-20, page 4 of the specification, i.e., the comparator only receives a detection voltage and cannot have a detection voltage) and that the number of cascode pairs is chosen based on the difference between the voltage to be detected and the reference detection voltage (see lines 6-16, page 6 of specification).

Claims 2-4, 6 and 7 are objected to because they include the above informalities of claim 1.

Also in claim 3, "wherein the comparator has a detection voltage level" on line 1 should be changed to --wherein the detection voltage level-- to avoid unclear antecedent basis of "a detection voltage level" which is already recited in claim 1.

Also in claim 3, line 2, "as" should be changed to --is--.

Appropriate correction is required.

*Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 3, this claim is indefinite because the formula/equation of the detection voltage level is not provided so it is not known how the detection voltage level is defined. Note that, the equation/formula was left out. Also, note that, if the same equation " $VBG \cdot (R2 + R3) / R3$ " in the original claim is used again, then it is not clear whether it is still true that the detection level is  $VBG \cdot (R2 + R3) / R3$  since that voltage level is only applied to the circuits in Figures 1 and 2 (applicant's admitted prior art), and the above equation/formula may not be able applies to the circuit in Figure 5 since there is a voltage drop across cascode transistors Q2A-Q2E (note that claim 1 was amended to include the cascode transistors). Clarification and/or appropriate correction is required.

With respect to claim 4, the recitation "the second comparison voltage has a voltage level that is within a range of the detection voltage level, thereby obtaining a required detection voltage level" on the last 3 lines is indefinite because it is not clear what exactly means by "within a range of the detection voltage level, thereby obtaining a required detection voltage level" (i.e., at what voltage level is considered to be within a range of the detection voltage level. Further, the detection voltage level is just a fixed voltage level, e.g. a predetermined voltage value such as 1.5V, 3V etc., and thus there is no upper and lower limits so it is not clear how a voltage can be considered as within a

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range". Further, "thereby obtaining a required detection voltage level" is also indefinite because it is not understood what voltage is that. Clarification and/or appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi (USP 5,814,995) in view of Fukami (USP 5,521,489).

Note that Figure 7 of the Tasdighi reference discloses a voltage detector circuit (R1-R3, 65, 66, 56), which includes a resistor pair (R2, R3) connected to an input voltage (voltage at the junction node of resistors R2 and R3); a reference resistor (R1) connected to one resistor (R2) of the resistor pair (R2, R3) for producing a first comparison voltage (node of connected to the positive terminal of 56); at least one transistor pair (65, 66) connected to the other resistor (R3) of the resistor pair (R2, R3) and the reference resistor (R1) for producing a second comparison voltage (node connected to the negative terminal of 56); and a comparator (56) for comparing the first comparison voltage and the second comparison voltage for outputting a voltage level (Vout). The voltage detector circuit in Figure 7 of does not discloses the voltage detector circuit further includes a number of cascode transistor pair(s) that is cascode to the at least one transistor pair. However, the Fukami reference discloses in Figure 4 a comparator circuit in comprising a plurality of cascode transistor pairs (42-43, Col. 2, lines 5-7) in which the first comparison voltage

(Va), the second comparison voltage (Vb), the difference of the first and second comparison voltage (Va, Vb) and the output voltage (Vout) are depending on the plurality of cascaded transistor pairs. Thus, it would have been obvious to one having skill in the art at the time the invention was made to modify the voltage detector circuit in Figure 7 of the Tasdighi reference by providing a number of cascode transistor pair(s) to the at least one transistor pairs (65, 66) for the purpose of setting the voltages of the voltage detector circuit to specific desired voltage levels for comparison, i.e., for detecting the input voltage (i.e., voltage to be detected) at a specific desired reference detection level. Thus, this combination/modification meets all the limitations of claims 1-4 and 6 because the structure of the combination/modification fully met the claims structure and substantially identical to applicant's invention (Figure 5), so all the functional limitations of claims 2-4 must also be met and of the functional limitation of claim 6 is also met as well, i.e., if the detection voltage level is twice as high as the second comparison voltage then the number of pairs would also be 2.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi (USP 5,814,995) in view of Fukami (USP 5,521,489), and further in view of Malhi (USP 5,731,686).

With respect to claim 7, above combination/modification (Tasdighi and Fukami) as discussed in claims 1-4 and 6 meets all the limitations of this claim except that the voltage detector circuit further includes the switch coupled between the resistor pair and the input voltage. However, the Malhi reference discloses in Figure 3 a circuit that including a switch (216) connected between reference node 214 and the input signal for switching the circuitry between the standby state and operation state. Thus, it would have

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been obvious to one having skill in the art at the time the invention was made to modify the voltage detector circuit in the above combination/modification (Tasdighi and Fukami) by providing a switch connected between the resistor pair and the input voltage as taught by the Malhi reference for the purpose controlling operational state and standby state of the circuitry and thus for saving the power consumption of the circuit because during a standby state, the switch would be off and thus no current can flow through the resistor pair. Thus, this modification/combination meets all the limitations of claim 7.

***Response to Arguments***

7. Applicant's arguments filed 7/11/05 have been fully considered but they are not persuasive.

With respect to the rejection under 35 U.S.C. 112, 2<sup>nd</sup> paragraph, claim 4 is still indefinite as discussed above. Note that the amendment also causes claim 3 to be indefinite as discussed above.

With respect to the rejection under 35 U.S.C 103, in response to applicant's arguments against the references (Tasdighi, Fukami, and Malhi) individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Further, applicant argues that Fukami cascode transistor pairs are FETs rather than BJTs. This argument is not persuasive because diodes 42 and 43 in Figure 4 of Fukami are formed by BJTs (see lines 5-7, Col. 2) because the collector and base of a transistor must exist in bipolar transistor (not FET).

Further, applicant argues that “Fukami teaches a variety of different temperature compensating elements including resistance 21 and diodes 34, which are not necessary in the claimed invention”. However, this argument is not persuasive because the purpose of using Fukami as the secondary reference in the combination/modification is to support that the voltages at the positive and negative terminals of the comparator depend on the number of cascode transistors, and thus the difference between the two comparison voltages (at the positive and negative terminals of the comparator) also depends on the number of cascode transistors. Note that, with the cascode transistors are provided in Figure 4 of Fukami, Fukami clearly stated that the difference of the voltage between the negative and positive terminal of the comparator is substantially zero (i.e., the two comparison voltages depend on the number of cascode transistors).

Applicant also argues that Malhi is actually controlled to provide a constant battery output voltage rather than power-saving power disconnection. However, this argument is not persuasive because when the switch off, then it is in standby state (see lines 45-46 and 64-65, Col. 4), and one skill in the art clearly understood that when the circuit is in a standby state (i.e., not operated) then the current is not flown through the circuit, so the does not does not consume power during standby state, and thus, switching to standby state will save power.

### ***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).



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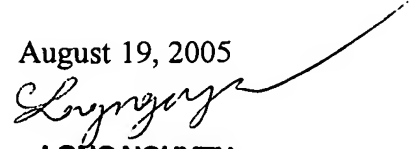
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:20am to 6:50pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 19, 2005

  
**LONG NGUYEN**  
**PRIMARY EXAMINER**